High dynamic Range High Sensitivity Readout Circuit for Infrared Focal Plane Array

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Introduction

The aim of HDR(high dynamic range) is to increase the dynamic range of luminosity. With the sacrificing of absolute accuracy, the chip can sense more intensity levels. We refer to the main concept and processing method of an ISSCC paper and design the circuit architecture in the pixel to achieve better performance.

A CMOS image sensor chip with 32 x 32 pixel array and 20 x 20μm^2 pixel size has been designed and fabricated in 0.18μm CMOS technology. The supply voltage is 3.3V. The chip area occupies 1.2mm x 1.2mm. It can achieve at most 40dB improvement of dynamic range in simulation.

Circuit architecture

Fig.1 The Pixel circuit

Fig.2 The timing diagram of control signals

Fig.3 Comparison diagram

Fig.4 The Correlated Double Sample circuit

Fig.1 shows the schematics of the circuit in the pixel. Based on the virtual shot property of opamp, "vin-" will be fixed at the same value as "vin+". We connect a photodiode to "vin-". When the photodiode is exposed to light, it forms photocurrent, which flows into the opamp. Cop is the integration capacitor, and it makes the op_output voltage decrease linearly. For different luminosity, the photodiode forms different amounts of currents and produces different output voltages.

Fig.2 shows the control signals of pixel. First, we reset every node to 2.5V by turning on all the switches in the pixel. After reset stage, the pixel goes through three different exposure periods with 5μs, 75μs, 1125μs individually. The ratio between three exposure periods is 1:n:n^2. The op_output voltage will decrease linearly in a period when exposed to light (the slope = dv/dt = iPD/Cop). Due to charge sharing between two exposure periods, the value of out becomes the average of op_output and 2.5V. Hence we can get greater dynamic range by synthesizing three images of different exposure periods.

In Fig.3, the red line, green line and purple line show the value of out for exposure time which are 5μs, 75μs and 1125μs, respectively. The blue line shows the ideal value of out after synthesis = 0.5*(0.5*(2.5+out_5μs)+out_75μs)+out_1125μs. In order to shorten the settling time, we add a PMOS to the circuit to let it reset faster. After three exposure periods, the circuit enters readout stage.

CDS(Correlated Double Sampling) is a useful method to reduce the influence of low frequency noise such as KTC noise and charge injection effect. Fig.5 shows the schematic of the CDS circuit. We use this method in the readout part of the chip.

First, the value of out will be sampled onto a capacitance by turning on SHS. Second, the value of reset will be sampled onto another capacitance by turning on SHR. After these two values are sampled, the clamp signal will turn on and the eq signal will turn off, causing the difference between voltage of out_s and out_r. The value of the difference is equal to the difference between voltage of reset and signal approximately.

Simulation result

The pre-layout simulation is based on the 5 x 5 pixel array. Fig.6 shows the waveform of the whole system. We derive the value of out from the waveform of CDS. Because the output swing range is from 2.5 to 0.6, there is some deviation when voltage of out is low.

Fig.7 shows the comparison diagram between post-sim for the pixel and ideal situation. Fig.8 is the microphotograph of the fabricated chip.