I. Abstract

III. Device Characteristics and Analysis

\[ LD = 4 \, \mu m, \quad a \]  
\[ LGD = 2 \, \mu m, \quad a \, \text{gate length} \, LG = 1 \, \mu m, \]  
\[ LGS = 1 \, \mu m. \]

II. Architecture

\[ \mu m \]